CS 102 Computer Organization and Architecture

Prerequisites : None

Course content:

Number System (5%)
Decimal, Binary, Octal, Hexadecimal, conversion from one system to another, binary arithmetic

Data Representation (10%)
Number representation, Addition of positive numbers, Addition and Subtraction of Signed Numbers, Overflow in Integer Arithmetic, Floating point representation, Floating point arithmetic, Character representation.

Combination Circuits (10%)
AND, OR, NOT, NAND, NOR, XOR gates, Boolean Algebra, Sum of Products, product of sum, K maps simplification, Don't care condition, Multiplexors, Demultiplexers, Decoders, Encoders

Arithmetic Circuits (10%)
Half Adder, Half Subtractor, Full adder, Full Subtractor, Ripple mode adder, Look ahead adder.

Sequential Circuit (10%)
Flip Flops, RS, Clocked RS, D, Edge triggered D, JK, T flip flop, counters, Shift registers, Multiplier circuits, booths multiplication, Divider circuit.

Basic Structure of Computers (5%)
Computer types, Von Neumann Architecture, Functional Units, Basic Operational Concepts, Evolution of Computers.

Instruction sequencing and Addressing Modes (15%)
Register Transfer Notation, Assembly language Notation, Basic Instruction types, Instruction Fetch and Execution cycle, Straight-Line Sequencing, Branching, Condition Codes, Generating Memory Addresses, one address, two address, three address and zero address instructions. Different addressing modes. Introduction to Assembly programming

Processing Unit (10%)
Fundamental concepts, Execution of a Complete Instruction, Multiple-Bus Organization, Hard-wired Control Unit, Micro programmed Control Unit.

The Memory System (10%)
Basic memory Concepts, Semiconductor RAM Memories, Read-Only Memories, Speed, Size and Cost, Caching, Directly mapped Cache, Associative mapping, Set Associative mapping, cache replace algorithms, Performance Considerations, virtual memory, secondary storage.

Pipelining (10%)
Basic Concepts, Data Hazards, Instruction Hazards, Control Hazards. Influence on Instruction Sets, Datapath and Control Considerations, Superscalar Operation, Performance Considerations.

Input/Output Organization (5%)
Accessing I/O devices, Interrupts, Programmed I/O, Interrupts driven I/O, Direct Memory Access.

Main Reading

1. C. Hamacher, Z. Vranesic and S. Zaky, "Computer Organization", fifth edition, 2002,McGraw-Hill Publication.

Supplementary Reading

1. Stallings W., "Computer Organization and Architecture" (7th edition) Prentice Hall of India, New Delhi
2. M. Morris Mano, "Computer System Architecture",(3rd edition) Prentice Hall of India, New Delhi